LDPC - Decoder On FPGA

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Introduction

Low-density parity-check (LDPC) code is a linear error correcting code used for transmitting messages over noisy transmission channels By applying a joint code and decoder design methodology, we have developed a high-speed (3, k)-regular LDPC code partly-parallel decoder architecture based on which we have implemented a 1152-bit (3, 6)-regular LDPC code decoder on a FPGA device.

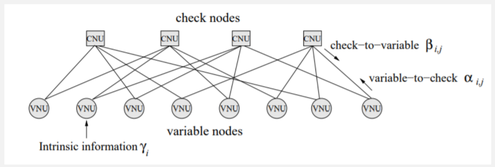
An LDPC code is defined as the null space of a very sparse M X N parity check matrix, and is typically represented by a bipartite graph , usually called as Tanner graph. There are N variable (or message) nodes in one set and M check (or constraint) nodes in another set in this graph. LDPC codes can be effectively decoded by the iterative BP or Belief-Propagation.

Software

We have mainly used **Verilog**, which is a hardware description language (HDL) for modelling electronic systems. It is the most commonly used in the design and verification of digital circuits at the register-transfer level of abstraction.For compilation and simulation,we have used open source iverilog compiler .

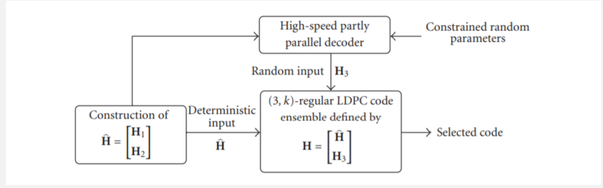
BP Algorithm

It is an iterative message passing algorithm. In each round of the algorithm, messages are passed from variable nodes to check nodes, and then back from check nodes back to variable nodes. Since the direct implementation of BP algorithm would have resulted in high hardware complexity due to a large number of multiplications, we have used logarithmic quantities to convert these multiplications into additions. This modification results in the Log-BP algorithm. Both BP and Log-BP algorithm realize the same decoding rule. Every decoding iteration can be performed in a fully parallel manner by mapping each check or variable node to one decoding processor as illustrated below.

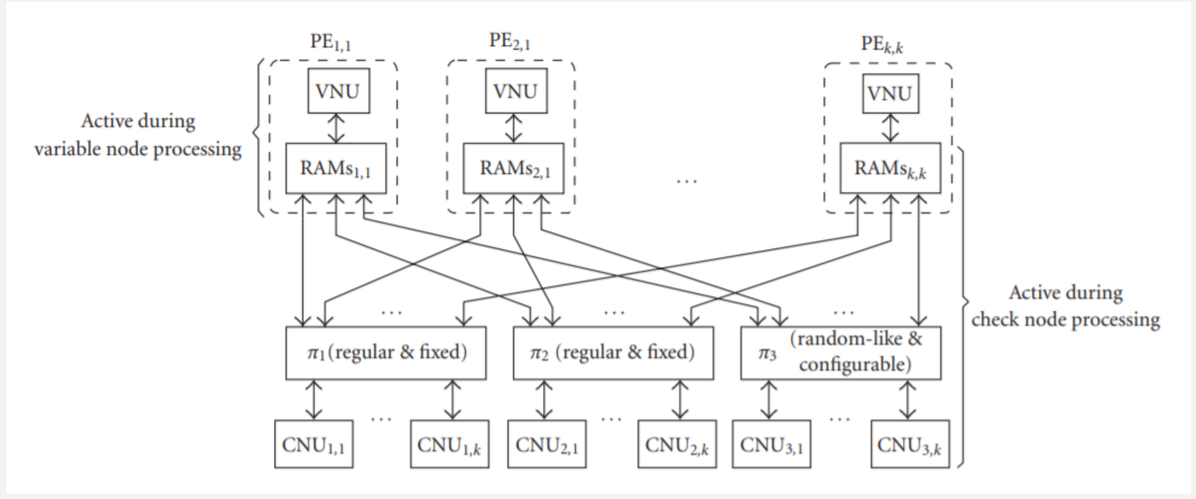


Methodology

Firstly we explicitly constructed a high-girth (2,k)- regular LDPC code that exactly fitted a high-speed partly parallel (2,k)-regular LDPC decoder. Then we extended this decoder to a (3,k)-regular LDPC decoder that was configured by a set of constrained random parameters. This defined a (3,k)-regular LDPC code ensemble. Each code in such an ensemble was constructed by randomly inserting certain check nodes into the deterministic high-girth (2,k)-regular LDPC code under the constraint specified by the decoder.



Architecture



Conclusion

Partly parallel decoder implementations provide appropriate trade-off between complexity and speed. Hence they are highly desirable for numerous applications. Due to the randomness of LDPC code construction, effective high speed partly parallel decoder design approaches turn out to be non trivial. We believe such joint design approach should be a key for practical LDPC coding system implementations. Future research work can be directed towards investigating the joint design approaches for the more general(j,k)-regular LDPC codes and irregular LDPC codes. The later one seems more promising from practical point of view.

References

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